An FPGA-based feedback control system that suppresses the nanoscale resonance

Chia-Feng Chang

NSRRC

101 Hsin-Ann Road, Hsinchu 300, Taiwan

donnychang@nsrrc.org.tw

Abstract- Controlling accuracy of an active optical systems employed in the beamlines needs to be better than nanometer. Piezo-translators that are capable of executing fast motion with high-precision and high loading are very suitable for this application. Most of the Piezo-based systems are executed in a closed-loop manner for high-precision and high stability. Yet, resonance phenomenon can still persist, dramatically degrading the system accuracy and stability. In this work, we report on using a 24 bits high-resolution data acquisition (DAQ) board to implement the PZT control to tackle the resonance phenomenon, instead of using hardware notch filter as commonly adopted in conventional Piezo-control system. FPGA system is designed in a closed-loop PID form. This system controls a bender constructed with two independent working PZTs, achieving the same effect as notch filter based control system. For example, under the working condition where the natural frequency of the bender is close to the operating frequency of the feedback loop, the PID operation still effectively inhibits the resonance phenomenon without a need to adjust manually the operating frequency as is often required for the notch filter design. This working scheme increases the convenience of the system application.

***Keywords*:** FPGA PZT Close-loop PID Beamline Real-Time

1. Introduction

Close-loop control system plays an important role in the control system. The quality of PID parameter and analog input/output system will affect the performance of the control system. This research aims at designing a control system which applies the analog input/output system and PID application. In the traditional PZT system, it uses Notch Filter to reduce the frequency and amplitude of noise. However, Notch Filter can only be adjusted manually and it needs to be adjusted every time thenoise frequency varies and thus is very inconvenient. To improve the stability of the PZT system and make it a more convenient tool, we use the high-resolution analog input/output system and the PID structure to design a control system; The high-resolution analog input/output system is capable of resolving the signal to nanometer-scale and is triggered by FPGA in a synchronized manner; adding PID mode and Bandstop filter function into such configuration, the stability of a PZT system is enhanced and the adjustment in response to different noise frequency becomes more convenient. As a result, the PZT system on the beamline is featured with high stability and better convenience.

2. System architecture

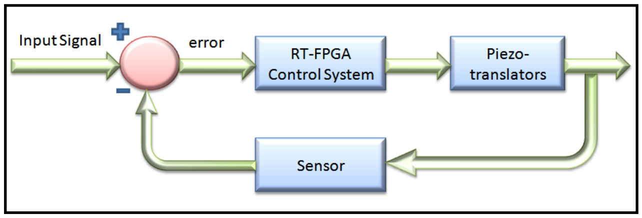


Fig. 1. Close-loop Control architecture of PZT control system

The control system configuration in this study uses RT close-loop control as the design. It applies high resolution analog input/output module and FPGA module as the reading and processing unit which comprised the hardware; while PID mode and Bandstop Filter combined forms the software and is used to process the signal. Besides, Piezo translators are the components that do the actual movement; the reading sensor is the HV Monitor in the PI system which feedback the analog signal of the real actuating condition to the Piezo translators Sensor.

2. 1. Control system description:

The control system described in this research can be divided into three parts. The first part is the computer-controlled core, including PXI-8108 multi-core controller facilitated with RT mode, 24Bits high resolution analog input/output module and FPGA module as hardware, and PID control mode and Bandstop Filter as software for signal processing. The hardware in this part is responsible for signal processing and data collecting and storage; the second part is the voltage amplifier module in the PI system which covert the analog output in the high resolution analog input/output module to high voltage and use the high voltage to connect to the Piezo translators in which the high voltage information is gathered by the internal sensor; the third part are the Piezo translators. Once they receive high voltage signal, they change lengths in response to the voltage ratio. And the information for length change can be derived from the Piezo translator sensor end.

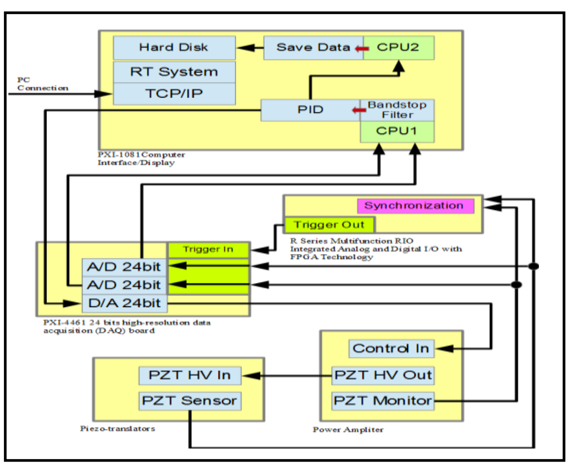


Fig. 2. System architecture of PZT control system

2. 2. System process flow:

After the system is turned on, RT system reads the voltage signal generated by the Piezo translator sensor and the voltage signal generated by the PI system module's Monitor via the high resolution analog input/output module; and then synchronize the two voltage signal using FPGA module to prevent the time error in the voltage signal. Next step is to eliminate noise frequency signal by Bandstop Filter. Once the external signal is processed and the Piezo translator length is fixed, use the first CPU set in PID mode for signal processing and the second CPU set to store each variables into the hard disk. Then the PID in the first CPU will generate voltage signal which leads to the change in the Piezo translator length. Repeat the process so that the PID in the system continuously makes adjustments.

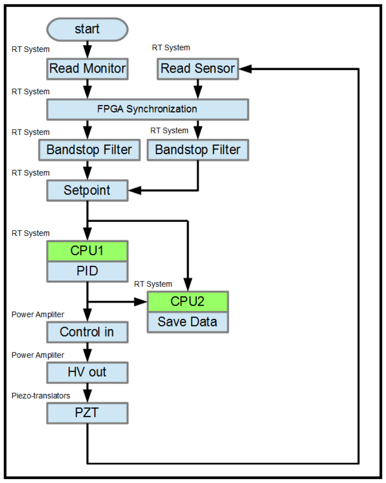


Fig. 3. Flow chart of PZT control system

2. 3. Hardware description:

High-accuracy data acquisition devices

The National Instruments 4461 is high-accuracy data acquisition devices specifically designed for sound and vibration applications. The devices include the hardware and software needed to make precision measurements with microphones, accelerometers, and other transducers that have very large dynamic ranges.

Fig. 4. The picture of high-accuracy data acquisition devices

FPGA Technology

NI R Series multifunction RIO devices offer the best combination of value and performance by integrating this FPGA technology with eight analog inputs, eight analog outputs, and 96 digital I/O lines, all into a single device that is offered on standard PC form PXI, Using the LabVIEW FPGA Module.

Fig. 5. The picture of FPGA Module

Piezo translator

P-245 preloaded PZT translators are high-resolution linear actuators for static and dynamic applications. They provide sub-millisecond response and sub-nanometer resolution.

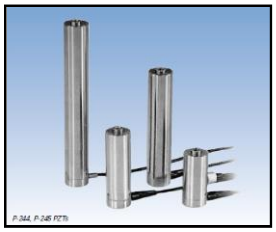


Fig. 6. The picture of PZT translators

2. 4. Program interface

Program interface applies National Instruments LabVIEW as the layout. One can acquire system information from the graph, including PID parameter, PZT sensor, analog output waveform and set point information; moreover, the content of the program is composed of PID construction, high resolution analog input/output module reading program, data storage, dual-core control, synchronize motion control, and Bandstop Filter program.

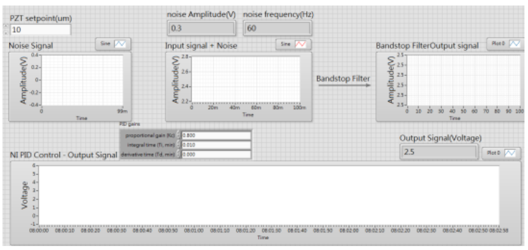


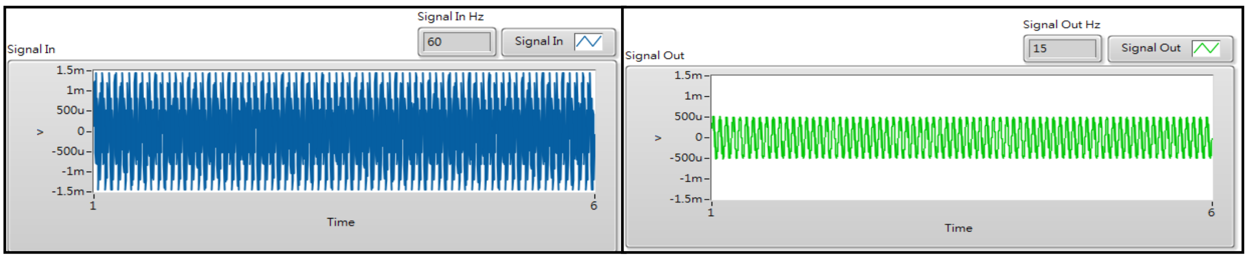
Fig. 7. The visual Control interface

2. 5. Test data

PZT oscillation

Piezo translators will generate noise depending on the environment it functions. If the signal is not filtered then signal error could arise, and will affect the accuracy of the system. Therefore, it is necessary to reduce the noise signal using filters, such as a Notch Filter. From the graph, it is obvious that the ±1.5mV noise signal will cause a variance of ±8nm if not passing a Notch Filter; however, when a Notch Filter is used, the noise signal is reduced to ±0.5mV which equals to a variance of ±3nm. Besides, re-adjustment of the Notch Filter has to be carried out once the system environment changes, and this can be very convenient. As a result, PID configuration is applied for analysis purpose.

PI Notch Filter

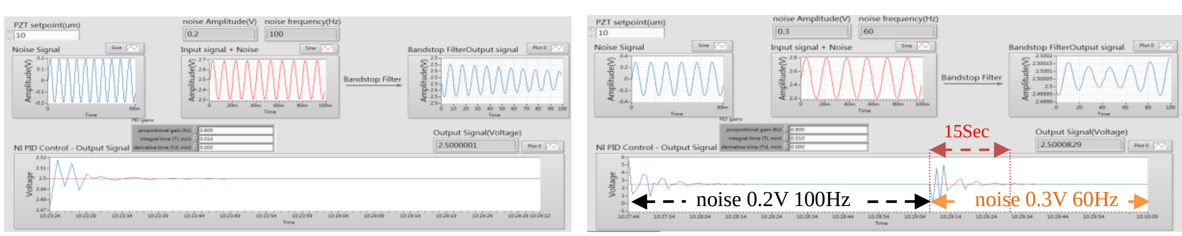


(a) (b)

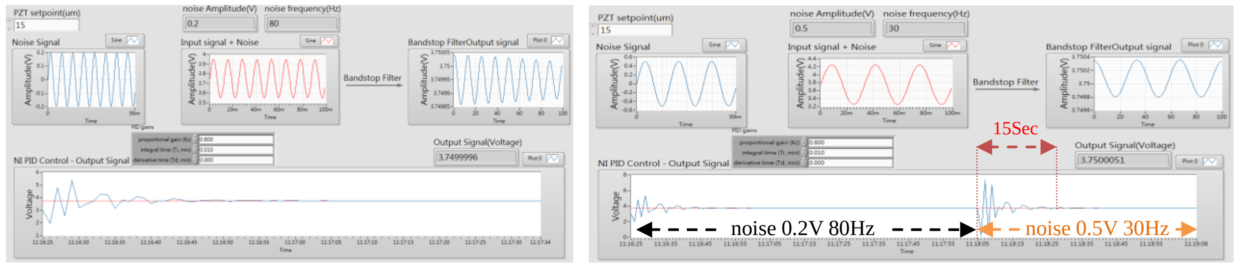
Fig. 8. Capture resonance signal of PI system (a) resonance error without Notch Filter (b) resonance error with Notch Filter

NI PID SYSTEM

To improve the stability and make it a more convenient tool, the application of NI LabVIEW PID is integrated with the Bandstop Filter which can reduce the influence from the noise while maintain the correctness of the signal in the meantime. In the following is the Piezo translator test at location 10μm and 15μm, respectively. Display in the graph indicates the change in the voltage waveform after PID processing. Apparently, when the 10um order is given, PID mode in the system starts to make adjustment. Because the starting voltage is the farthest to the targeting voltage, the rise in voltage is the largest. Then use the smallest voltage to adjust. Currently the signal adjustment is rather small; hence, the output signal gets smoother and the overall system functions in a stable condition. In the steady state, if there is a resonance effect occurs, the system need to be stabilized Piezo translators, will adjust its output voltage to a steady state.



(a-1) noise 0.2V,100Hz (a-2) noise 0.3V ,60Hz ,Response time<15Sec



(b-1) noise 0.2V 80Hz (b-2) noise 0.5V, 30Hz, Response time <15Sec

Fig. 9. The output voltage signal of NI PID control system. (a) The set point at 10μm with noise (b) The set point at 15μm with noise

Table. 1. Test data on table

PZT	Set Control Out (V)	PV stability voltage	PZT length	Response time
10μm	2.5V	±10μV	±0.05nm	< 15sec
15μm	3.75V	±10μV	±0.05nm	< 15sec

3. Conclusion

FPGA hardware module can gather different signal and then process the signal. Furthermore, it can be integrated with the high resolution analog input/output module and can be combined with RT system. On the other hand, software applies PID mode and Bandstop Filter mode to reduce the effect of the noise. This can enhance the stability of the Piezo translators to nanometer-scale and makes the adjustment of the noise effect more convenient. In sum, the system described in this study improves the stability of the beamline control and makes the adjustment become more convenient; besides, the RT-FPGA system can reduce the signal error caused by time delay and thus enhance the correctness of signal processing.

Acknowledgements

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